



4. ELECTRICAL PERFORMANCE						
4-1. Video system characteristics						
		Specification				
	Parameter	min	typ	max	unit	Remark
4-1-1	Input impedance			1.3	K	measure at 0.5 ~ 5 MHz
4-1-2	Input signal level			1	Vp-p	load of 92 ohm connected negative synchronous
4-1-3	Modulation fp 2480 MHz (sine wave 300KHz 1Vp-p)	2	3	4	MHz	Superimposed sinuous wave (2.58 MHz) is 20% of the step input level. Measure with under the APL of 10~90% differential gain of demodulator unit is to be compensated..
4-1-4	Differential gain	8		8	%	
4-1-5	Differential phase	-8		8	deg	-ditto-
4-1-6	S/N	45			dB	Measure with respect to standard demodulator output.
4-1-7	Out level taper		4	6	dB	Fp 2400~2483mhz.
4-2. Audio system characteristics						
4-2-1	Input impedance		1.4		Kohm	Measure at 0.1-10khz
4-2-2	Modulation	35	40	45	khz	
4-2-3	Distortion factor			3	%	Audio input signal 1.0Vp-p 1khz modulation 50% (sine wave). Video input signal all black (sync.only) use standard demodulator of inter-carrier system. De-emphasis(50 usec) is on.
4-2-4	S/n	40			dB	



4-3. Output system characteristics							
Parameter		Specification.				Remark	
		min	typ	max	unit		
4-3-1	Video carrier frequency	-50	fp	+50	KHz	Test at 25°C temperature and 65% RH of humidity Fp 2400~2483 Mhz Fs1 6.5 mhZ Fs2 6.5 mhz *output channel	
4-3-2	Video output level	13	14	16	dBm		
4-3-3	Audio output level difference(P/S ratio)	22	27	32	dB		
4-3-4	Audio carrier frequency	-8	fs	+8	KHz	Input signal none the measurement is taken after 30 sec. from the power-on.	
4-3-5	Audio modulator fs1 fs2	35	50	65	KHz	Measurement difference video of carrier frequency output level for 2400~2483 Mhz except to fp. fp+/-fs against video carrier output level.	
		35	50	65			
4-3-6	Out-band spurious	50	55		dB		
4-3-7	In-band spurious within bandwidth	60			dB		
4-3-8	Output impedance		75		ohm		
Unbalanced.							



5-1. PLL section characteristics												
No	Item	Specification									notes	
5-2.	(1) SDA SCL input voltage	Under standard test condition									V	
		Condition	Min	Typ	Max							
	High voltage	3		5								
	Low voltage	0		1.5								
	(2) Address	C2 (on write date format)										
	(3) SDA SCL input impedance	SDA/SCL are in the high impedance and there should be no reliability problem with 5V continually on the SDA/SCL, if power supply is switched off.										
	(4) Data format	MSB					LSB					
	Address	1	1	0	0	0	MA1	MA0	0	A	Byte1	
	Programmable Divider	0	2	2	2	2	2	2	2	A	Byte2	
	Programmable Divider	7	6	5	4	3	2	1	0	A	Byte3	
	Charge pump and test bits	1	(0) CP	T1	T0	1	1	1	(0) os	A	Byte4	
	I/O port control bits	P7	P6	P5	P4	P3	P2	P1	P0	A	Byte5	
	Table 1 write data format (MSB is transmitted first)											
	Address	1	1	0	0	0	Ma1	Ma2	1	A	Byte1	
	Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte2	
	<p>Table 2 read date format</p> <p>A: acknowledge bit.</p> <p>Ma1, Ma0: voltage address bits.</p> <p>CP: charge pump current select.</p> <p>T1: test mode selection, T0: charge pump disable</p> <p>OS: varactor drive output disable switch.</p> <p>P7, P6, P5, P4, P3, P2, P1, P0: control output states</p> <p>POR: power on reset indicator</p> <p>PL: phase lock detect flag</p> <p>I2, I1, I0: digital information from ports P7, P5, and P4.</p> <p>A2, A1, A0: 5 level ADC data from P6</p>											

